Amendments to the Claims:

Please cancel claims 1-12 and add the following new claims:

13. (new) A dense memory cell comprising:

a plurality of access transistors, each having a gate tied to a wordline input, a first one of the access transistors having a drain and source coupled between a bit line and an output node;

a plurality of storage transistors, a first one having a drain and source coupled between the output line and a power signal and a gate couple to an output bar node, the second one having a drain and source coupled between the output bar node and the power rail, and a gate coupled to the output node; and

a control circuit generating a tracking voltage coupled to the wordline, the track voltage for adjusting the voltage on the wordline to cause leakage current through the two access transistors to exceed leakage through the plurality of storage transistors.

14. (new) The memory cell of claim 13 wherein the tracking voltage is a function of a reference voltage determined to provide a leakage through the access transistors that exceeds the leakage through the storage devices.

15. (new) The memory cell of claim 14 wherein the tracking voltage is maintained substantially constant by a differential amplifier.

16. (new) The memory cell of claim 15 wherein the tracking voltage is buffered to substantially reduce disturbances to VREF resulting from switching states on the wordline.

17. (new) The memory cell of claim 15 wherein the tracking voltage is generated by a reference circuit, the reference circuit comprising:

a plurality of partial memory cells, each partial memory cell comprising one access transistor and storage transistor configured in a worst case leakage condition; and

a differential amplifier having a voltage reference input and a second input coupled to an output node of each of the partial memory cells, the output of the differential amplifier being the tracking voltage.

18. (new) The memory cell of claim 13 wherein the tracking voltage is coupled to an N-well comprising storage transistors.

19. (new) The memory cell of claim 13 wherein the tracking voltage is coupled to the V_{ss} connection to which the storage transistors are coupled.

20. (new) A method of maintaining a preferred leakage ratio between access and storage devices in a memory cell, said method comprising:

establishing a reference voltage that is equal to a desired output voltage of the cell;

generating a tracking signal required to force the reference voltage onto an output of a dummy circuit; and

coupling the tracking signal to a point in the memory cell wherein a leakage current is generated in each of the access and storage devices and further wherein the leakage current in the access devices is greater than the leakage current in the storage devices.

21. (new) The method of claim 20 further including varying the well to substrate bias voltage of the storage devices to decrease the leakage through the storage devices.

22. (new) The method of claim 20 wherein the control signal biases the supply rail voltage to which the storage devices are directly coupled to decrease the amount of leakage through the storage devices.

23. (new) The method of claim 20 wherein a differential amplifier detects when the output state of a plurality of dummy cells have fallen below a predetermined reference voltage.

24. (new) The method of claim 23 wherein the differential amplifier generates the control signal at a level required to restore the output state to at or near the reference voltage.

25. (new) A dense memory cell comprising:

a plurality of access transistors, each having a gate tied to a well bias input, a first one of the access transistors having a drain and source coupled between a bit line and an output node;

a plurality of storage transistors, a first one having a drain and source coupled between the output line and a power signal and a gate couple to an output bar node, and a second one having a drain and source coupled between the output bar node and the power signal, and a gate coupled to the output node; and

a control circuit generating a tracking voltage coupled to the well bias, the track voltage for adjusting the voltage on the well bias during an idle state to ensure that leakage current through the two access transistors exceeds the leakage through the two storage transistors where the output node to which it is coupled is at VDD.

26. (new) The memory cell of claim 25 further comprising a tracking circuit that comprises a number of half configured memory cells that are placed in a state which mimics the stored state in a normal memory cell that would degrade during the idle state.

27. (new) The memory cell of Claim 26 wherein the track voltage is a function of a reference voltage determined to provide a leakage through the storage transistors that is less than the leakage through the access devices.